Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] An integrated circuit that integrates a plurality of functional blocks within a single semiconductor chip, comprising:
a plurality of decoding circuits within said semiconductor chip, for which address lines and data lines are connected to an input terminal, an address signal inputted from said address lines is decoded, and the data inputted from said data lines is outputted according to the results of the decoding; and
signal lines with a few bits including said address lines and said data lines, wherein said signal lines are wired to said plurality of the decoding circuits.

[c2] The integrated circuit according to claim 1, wherein said plurality of the decoding circuits are arranged in the same number of said plurality of functional blocks.

[c3] The integrated circuit according to claim 2, wherein said plurality of the decoding circuits are respectively arranged near said plurality of functional blocks.